bc988VME
Time Distribution Module

User's Guide
December, 1996

CHAPTER ONE
INTRODUCTION

1.0 GENERAL

The bc988VME Time Distribution Module User's Guide provides the following information:

- General Introduction and Overview.
- Installation Details.
- Software Interface Details.
- Input/Output Signal Information.
- Drawing Set.

1.1 FEATURES

The salient features of the bc988VME Time Distribution Module include:

- 8 X 8 crosspoint switch matrix.
- 75Ω driver on board for each of eight outputs.
- Each output has independent front panel gain control with front panel test points for monitoring output levels.
- Fault-protected inputs can withstand a continuous ±35V.
- Front panel and P2 connections for inputs and outputs.
- The 8 inputs can be daisy-chained to multiple modules to produce matrices of 8 X 16, 8 X 24, 8 X 32, etc.
- Current limited output protection.
- Uses 256 bytes in the VMEbus short address space. Can be freely located on any 256 byte boundary. A16:D08(O).

1.2 OVERVIEW

The bc988VME Time Distribution Module is an 8x8 cross point switch matrix with adjustable gain output drivers. The module is controlled via registers written and read over the VMEbus. By bussing the eight inputs to multiple bc988VME modules, the switch matrix can be expanded (e.g., 4 modules allows for an 8x32 switch matrix). The gain adjust pots are front panel accessible. Input and output connections are available on both the front panel and on the VMEbus P2 connector. Table 1-1 lists the principle performance specifications for the module.

Table 1-1
bc988VME Performance Specification

Item	Specifics	Description
Signal I/O	Input Amplitude	0.0 Vpp to 20 Vpp (protected to ± 30V).
	Output Amplitude	0.0 Vpp to 20 Vpp into 10kΩ.
	Output Drive	4.0 Vpp into 75Ω.
	Bandwidth	100kHz.
	Adjustable Voltage Gain	0 to 30.
	Input Impedance	1 Meg Ω.
	Output Impedance	75Ω.
	Switch Matrix	8 by 8.
	Switch Operation	Break Before Make.
VMEbus Interface	Standardization	Revision C.1 of the VMEbus Spec.
	Address Space	A16, AM Codes $29 and $2D.
	Data Transfer	D08(O).
	Power	+ 5VDC @ 800 mA. ± 12VDC @ 100 mA.
Operating and Storage Environment	Operating	0°C to 70°C.
	Non-Operating	-50° C to 125°C.

CHAPTER TWO
INSTALLATION

2.0 GENERAL

The bc988VME is a dual height (6U) VMEbus board designed to be installed in a standard VMEbus subrack. The module is mapped into the VMEbus A16 short address space and uses odd byte (D08[O]) data transfers. The bc988VME responds to address modifiers $2D (Short Supervisory Access) and $29 (Short Non-Privileged Access). This chapter details the steps required to install and setup the module in the subrack.

2.1 BASE ADDRESS SELECTION

Before installing the module in the subrack the address select DIP switch (U29) must be set. The bc988VME occupies 256 bytes in the VMEbus short address space and can be freely located on any 256 byte boundary. The eight DIP switch positions of U29 correspond to address bits A15 - A08 as shown in Figure 2-1 and determine the base address for the module. The base address is defined as the address selected by the U29 DIP switch when A07 - A01 are 0.

	DIP Switch U29							
Address Bit	A15	A14	A13	A12	A11	A10	A09	A08
U29 Switch	8	7	6	5	4	3	2	1

To select a base address, set each of the eight DIP switches to the ON (same as CLOSED) or OFF (same as OPEN) position. Setting a DIP switch to the ON position selects a logical 0 (zero) for the address bit. The OFF position selects a logical 1 (one).

CHAPTER THREE

SOFTWARE INTERFACE

3.0 GENERAL

The bc988VME Time Distribution Module is mapped into the VMEbus A16 short address space, and uses odd byte (D08(O)) data transfers. The bc988vme responds to address modifiers $2D (Short Supervisory Access) and $29 (Short Non-Privileged Access). This chapter describes the bc988VME control registers.

3.1 CONTROL REGISTERS

The crosspoint switch matrix is controlled via four (eight-bit) read/write registers accessible over the VMEbus. The base address of the bc988VME is set with an eight position dip switch as shown in Chapter Two. Each output channel uses four bits for its control, three bits determine the input source and one bit turns the output on or off. All registers are cleared to 0 (zero) when a VMEbus SYSRESET* is asserted.

The four D8(O) register locations are mapped redundantly in the 256 byte address range. The bc988VME register map is shown in Table 3-1. A logical 0 (zero) turns the channel output off; a logical 1 (one) turns the channel output on (bits D3 and D7). The channel source select bits (D0-D2 and D6-D4) are binary coded where 000 selects input 1 and 111 selects input 8.

Table 3-1
bc988VME Register Map

Offset	D7	D6 - D4	D3	D2 - D0
1	CH2 ON/OFF	CH2 SOURCE	CH1 ON/OFF	CH1 SOURCE
3	CH4 ON/OFF	CH4 SOURCE	CH3 ON/OFF	CH3 SOURCE
5	CH6 ON/OFF	CH6 SOURCE	CH5 ON/OFF	CH5 SOURCE
7	CH8ON/OFF	CH8 SOURCE	CH7 ON/OFF	CH7 SOURCE

CHAPTER FOUR

INPUT/OUTPUT CONNECTIONS

4.0 GENERAL

The bc988VME provides both front panel and P2 input/output connections. The front panel provides access to the gain adjust pots and output test points.

4.1 INPUT/OUTPUT CONNECTORS

The pinouts for the front panel 40 position IDC connector (J1) and the VMEbus P2 connector are listed in Table 4-1 (inputs) and Table 4-2 (outputs). J1 pinouts are setup with odd pins on one row and even pins on the opposite row.

Table 4-1
J1 and P2 Input Pinput

J1	P2	Signal
31	C2, C13	Input 1 Signal.
32	A2, A13	Input 1 Ground.
29	C3, C14	Input 2 Signal.
30	A3, C14	Input 2 Ground.
27	C4, C15	Input 3 Signal.
28	A4, A15	Input 3 Ground.
25	C5, C16	Input 4 Signal.
26	A5, A16	Input 4 Ground.
23	C6, C17	Input 5 Signal.
24	A6, A17	Input 5 Ground.
21	C7, C18	Input 6 Signal.
22	A7, A18	Input 6 Ground.
19	A8, A19	Input 7 Signal.
20	A8, A19	Input 7 Ground.
17	C9, C20	Input 8 Signal.
18	A9, A20	Input 8 Ground.

Table 4-2
J1 and P2 Output Pinout

J1	P2	Signal
15	C24	Output 1 Signal.
16	A24	Output 1 Ground.
13	C25	Output 2 Signal.
14	A25	Output 2 Ground.
11	C26	Output 3 Signal.
12	A26	Output 3 Ground.
9	C27	Output 4 Signal.
10	A27	Output 4 Ground.
7	C28	Output 5 Signal.
8	A28	Output 5 Ground.
5	C29	Output 6 Signal.
6	A29	Output 6 Ground.
3	C30	Output 7 Signal.
4	A30	Output 7 Ground.
1	C31	Output 8 Signal.
2	A31	Output 8 Ground.

4.2 GAIN CONTROL POTS AND OUTPUT TEST POINTS

The channel gain control pots are located on the bc988VME front panel, one pot per output channel. The pots are labeled “CH1” to “CH8” and required a slotted screw driver or other adjustment tool. To increase the channel gain turn the pot clockwise.

Output test points are also located on the front panel. These test points allow you to monitor the output level while adjusting the channel gain. The test point jacks labeled “TP1” through “TP8” correspond to output channels 1 through 8, respectively. The test point jacks require standard 0.080” test plugs. A single ground test point label “TPG.” is located below TP8.

CHAPTER FIVE

THEORY OF OPERATION

5.0 THEORY OF OPERATION

The bc988VME circuitry consists of the VMEbus interface, the control registers, cross point switch multiplexers, and variable gain output amplifiers.

The VMEbus interface allows the control registers to be written and read. VMEbus data is routed through bi-directional buffer U44. A data transfer takes place when the VMEbus address modifiers (AM0-AM5) are equal to $29 or $2D as decoded by PAL U43, or the VMEbus address bits (A15-A08) are equal to the U29 dip switch setting as compared by comparator U41. When the address and modifier bits are set, signal ADEN* out of U43 is asserted low signaling the U35 interface chip to begin the data transfer. The 8-bit latch U42 latches address bits A07-A01 and the IACK* signal on the falling edge of AS*. A control register is selected based on the state of VMEbus address bits A01-A02 as decoded by the U34 decoder. The duration of the data transfer is determined by the U36 PAL which counts 4 SYSCLK (16 MHz) clock cycles before asserting the ACK* signal low which tells the interface chip U35 to complete the data transfer by asserting DTACK* low. DTACK* remains low until the data strobe signal DS0* is deasserted high. The VMEbus WRITE* signal determines whether the control registers are being read or written. When WRITE* is low, a control register is being written.

Control registers U25-U28 hold the input source select data. These 8-bit latches are clocked by the output of the U34 decoder during a write cycle. The latches are cleared when the VMEbus SYSRESET* signal is asserted low. Tri-state buffers U21-U24 are enabled during read cycles. These buffers allow the state of the control registers to be read over the VMEbus.

The eight input source signals are routed to eight 8-to-1 analog multiplexers (MAX358.) These muxes makeup the 8 x 8 cross point switch matrix. The output of the control registers are routed directly to the control inputs of the muxes. The input and output signals are routed to and from the P2 connector.

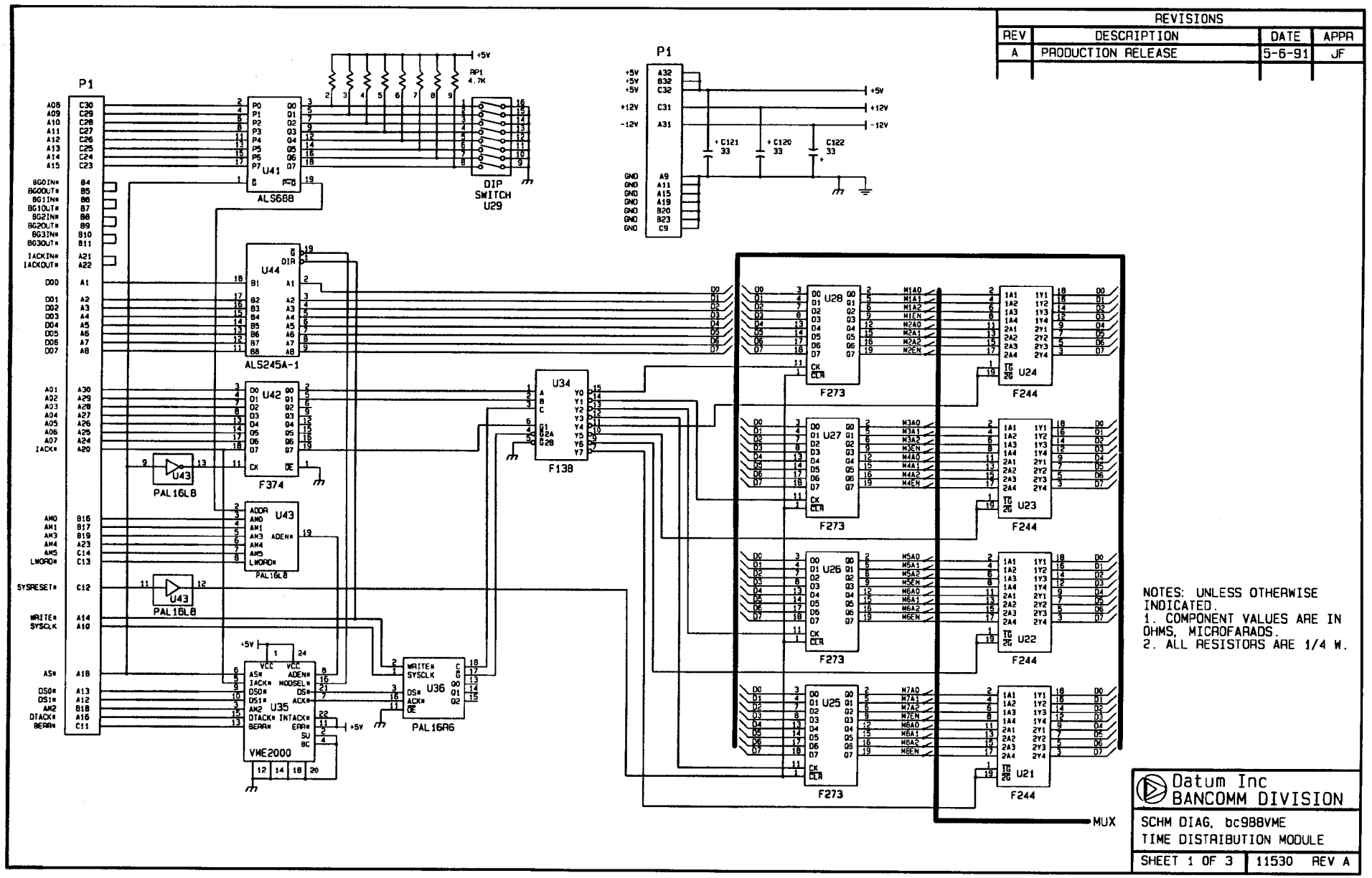
The output of the muxes are routed to the adjustable gain output amplifiers. The first stage of the amplifier section is a follower amplifier which is used to provide a high impedance input to the rest of the gain block. The follower output is sent to the adjustable gain amplifier which has a gain range of 0 to 5. The adjustable gain amplifier output is sent to a fixed gain (gain of 6) output drive amplifier resulting in an overall voltage gain range of 0 to 30. The test points are connected through a 10KΩ resister to the amplifier outputs.

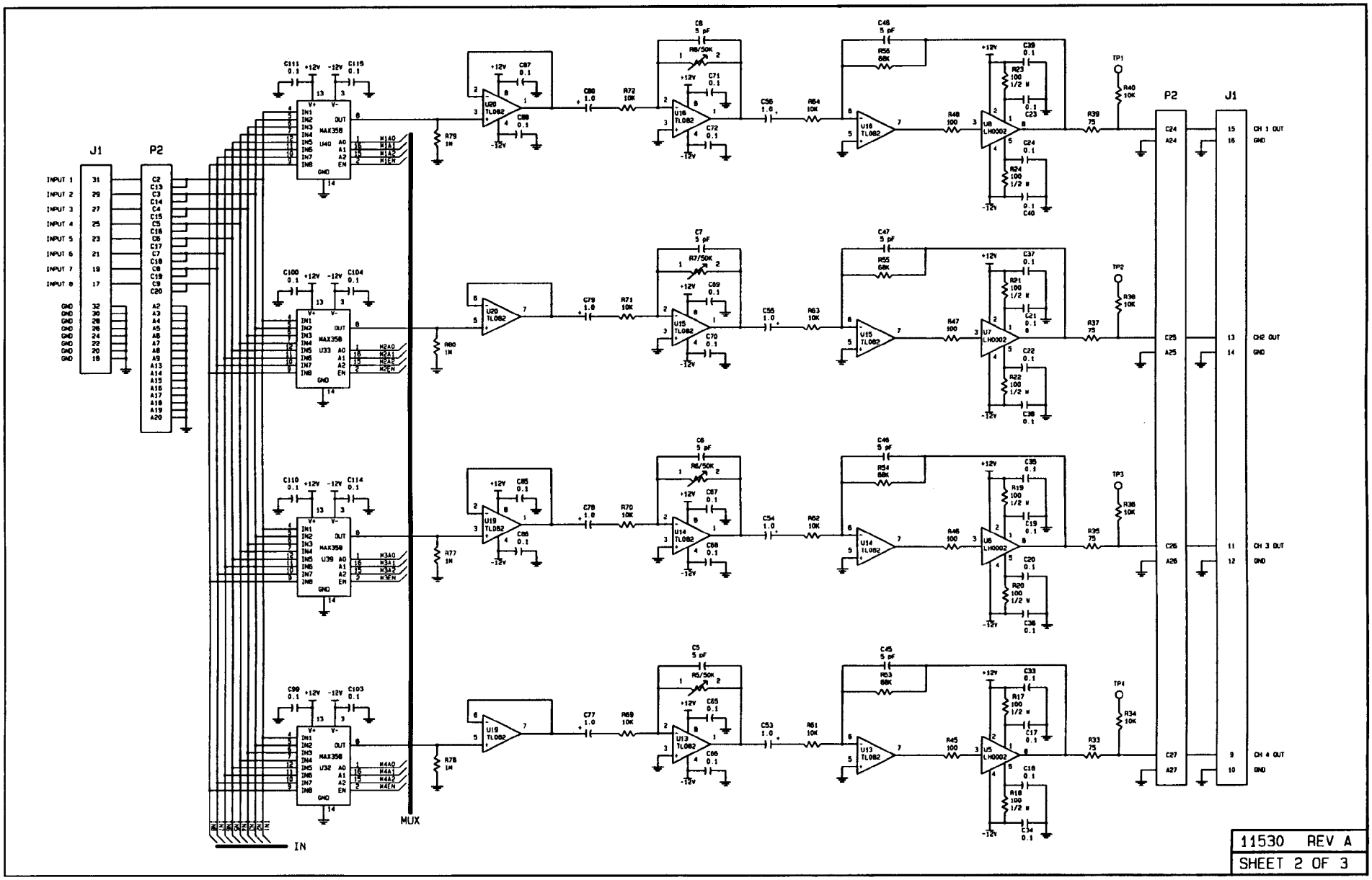
CHAPTER SIX
DRAWING SET

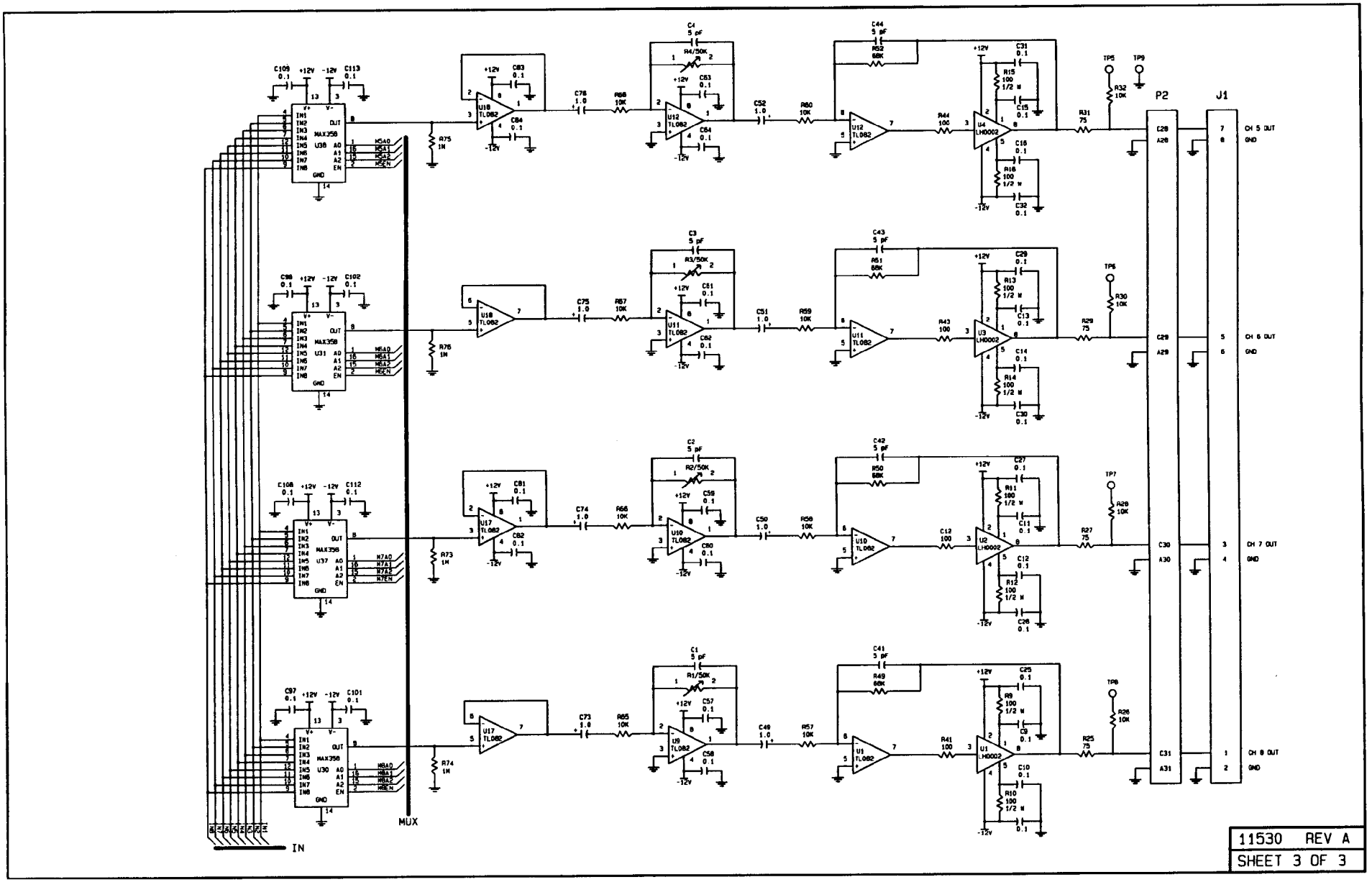
6.0 GENERAL

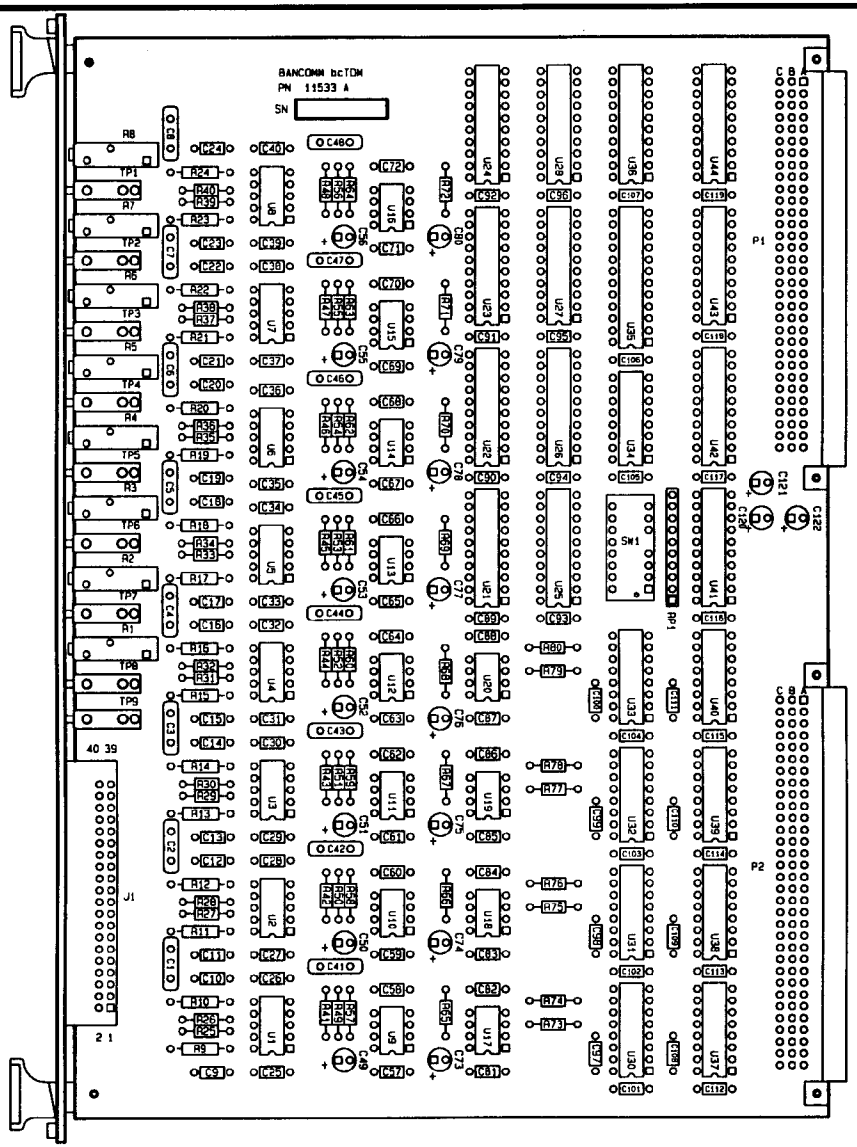
This chapter contains the drawing set for the bc988VME Time Distribution Module.

Drawing Number	Drawing Title
11530	Schematic Diagram.
11533	Assembly and Parts List.


REVISIONS
REV | DESCRIPTION | DATE | APPR
A | PRODUCTION RELEASE | 5-6-91 | JF
P1
RP1 4.7K
U41
ALS688
DIP SWITCH U29
U44
ALS245A-1
U42
F374
U43
PAL16L8
U34
F138
U28
U27
U26
U25
F273
U24
U23
U22
U21
F244
U35
VME2000
U36
PAL16A6
+5V
+12V
-12V
C121 33
C120 33
C122 33
MUX
NOTES: UNLESS OTHERWISE INDICATED.
1. COMPONENT VALUES ARE IN OHMS, MICROFARADS.
2. ALL RESISTORS ARE 1/4 W.
Datum Inc
BANCOMM DIVISION
SCHM DIAG, bc988VME
TIME DISTRIBUTION MODULE
SHEET 1 OF 3
11530 REV A


J1
P2
INPUT 1
INPUT 2
INPUT 3
INPUT 4
INPUT 5
INPUT 6
INPUT 7
INPUT 8
GND
MAX358
TL082
LH0002
MUX
IN
CH 1 OUT
CH 2 OUT
CH 3 OUT
CH 4 OUT
11530 REV A
SHEET 2 OF 3


P2
J1
MUX
IN
11530 REV A
SHEET 3 OF 3



REVISIONS			
LTR	DESCRIPTION	DATE	APVD
A	FIRST RELEASE	06/05/91	J.F.

UC170 FILE: A988_A1.SCH	Datum Inc BANCOMM DIVISION	
DRWN BY: JWL	ASSEMBLY, bc988VME	
DATE: 06/05/91	TIME DISTRIBUTION MODULE	
APP. BY: JF	SHEET: 1 OF 2	11533-A

Assembly, Parts Listing
bc988VME Time Distribution Module

Ref: Drawing No: 11533 A

Ref: UC 170

June 5, 1991

AS	OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
		1501050	CM05CD05D03	GI	5 PF, 500V	DIPPED MICA CAPACITOR	16.00	C1-8,41-48
		1503336	336RMR025M	IC	33 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	3.00	C120,121,122
		1504105	196D105X9035HA1	SPRAGUE	1.0 MF, 35V	TANTALUM CAP, RADIAL LEADS	16.00	C49-56,73-80
		1515104	MD015E104MAA	AVX/67349	0.1 MF, 50V	DIP GUARD CAPACITOR	87.00	C9-40,57-72,81-119
		2104001	913346	ERNI	96 POS	DIN CONNECTOR, MALE	1.00	P1,2
		2150020	10620-01-445	ANDON/SPECIRA	20 POS	DIP SOCKET	2.00	REF: U36,43
		2155003	040.111	SCHURTER		PCB MNT TEST POINTS	7.00	TP1-7
		2401610	11536A	DATUM INC. BC	bc988VME	FRONT PANEL	1.00	FP
		2404600	VME-6U-1450	PHILLIPS COMPONENT		VME EXTRACTOR HANDLES KIT	1.00	BKT1
		4701101	RC07GF101J	ALLEN BRADLEY	100 OHM, 1/4W	FIXED RESISTOR	8.00	R41-48
		4701103	RC07GF103J	ALLEN BRADLEY	10 K OHM, 1/4W	FIXED RESISTOR	24.00	R26,28,30,32,34,36,38,40 57-72
		4701105	RC07GF105J	ALLEN BRADLEY	1 MEG OHM, 1/4W	FIXED RESISTOR	8.00	R73-80
		4701683	RC07GF683J	ALLEN BRADLEY	68 K OHM, 1/4W	FIXED RESISTOR	8.00	R49-56
		4701750	RC07GF750J	ALLEN BRADLEY	75 OHM, 1/4W	FIXED RESISTOR	8.00	R25,27,29,31,33,35,37,39
		4702101	RC20GF101J	ALLEN BRADLEY	100 OHM, 1/2W	FIXED RESISTOR	16.00	R9-24
		4704503	3006P1-503	BOURNS	50K OHM, 1/2W	POTENTIOMETER	7.00	R2-8
		4705472	710A472	ALLEN BRADLEY	4.7 K OHM, 1/8W	C-SIP RESISTORS, 10 PIN 'X'	1.00	RP1
		5108002	76SB08	GRAYHILL		8PST DIP SWITCH	1.00	U29
		9004832	74F138	NATIONAL	16P DIP PKG	1-OF-8 DECODER/DEMUX	1.00	U34
		9006858	MM74F374N	NATIONAL	20P DIP PKG	OCTAL D FLIP FLOP	1.00	U42
		9013851	74F273	NATIONAL	20P DIP PKG	8 BIT SHIFT REGISTER	4.00	U25-28
		9015940	SN74ALS688N	TI	20P DIP PKG	8 BIT MAGNITUDE COMPARATOR	1.00	U41
		9201035	MAX358CP	MAXIM	16P DIP PKG	8 CHANNEL ANALOG MUX	8.00	U30-33,37-40
		9207815	74F244	NATIONAL	20P DIP PKG	OCTAL BUFFER/LINE DRIVER	4.00	U21-24
		9207920	SN74ALS245A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	1.00	U44
		9211001	VME2000-45	PLX TECHONLOGY	24P DIP	VME SLAVE INTERFACE	1.00	U35
		9306005	LH0002CN	NATIONAL	10P DIP PKG	CURRENT AMPLIFIER	8.00	U1-8
		9306035	TL082	TI	08P DIP PKG	DUAL BIPOLAR JFET OP AMP	12.00	U9-20
		9405015	PAL16L8B	MMI	20P DIP PKG .3W	PAL	1.00	U43
		9405025	PAL16R6A	MMI	20P DIP PKG .3W	PAL	1.00	U36
	001		11539B	DATUM INC. BC	bc988VME TDM	SPECIAL FRONT PANEL, AEROJET	1.00	FP
	001	2114020	3575-0000	3M	20 POS	BACKPLANE SOCKET	2.00	P2 A2,A22
	001	2117061	TSW-130-07-G-D	SAMTEC	2X30 POS	STRAIGHT TERMINAL STRIP	2.00	P2 A2,A22
	001	2120015	8315-6063	3M	15 POS	'D' SOCKET	2.00	J2,3 FP
	001	2802002	3341-1S	3M		JACK SCREW KIT	2.00	J2,3
	001	4701152	RC07GF152J	ALLEN BRADLEY	1.5 K OHM, 1/4W	FIXED RESISTOR	1.00	R1
00					bc988VME	STANDARD ASSEMBLY	0.00	
00		2104001	913346	ERNI	96 POS	DIN CONNECTOR, MALE	1.00	P2
00		2109040	3595-5002	3M	40 POS	RTANG HEADER	1.00	J1
00		2155003	040.111	SCHURTER		PCB MNT TEST POINTS	2.00	TP8,9
00		2401610	11536-A	DATUM INC. BC	bc988VME	bcTDM FRONT PANEL	1.00	FP
00		4704503	3006P1-503	BOURNS	50K OHM, 1/2W	POTENTIOMETER	1.00	R1